Analysis of higher order pitch division for sub-32nm lithography

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ABSTRACT

The three knobs of optical lithography, namely process factor k_1, wavelength (λ) and numerical aperture (NA) have been constantly pushed to print smaller features. To get an equivalent k_1 value below the fundamental limit of 0.25, double patterning (DP) has recently emerged as a viable solution for the 32nm lithography node. Various DP techniques exist such as litho-etch-litho-etch (LELE), litho-freeze-litho-freeze (LFLF) and self-aligned sidewall spacer. In this paper, the potential of higher order pitch division (pitch/N, N>2) for sub-32nm lithography is analyzed. Compared to double patterning, higher order pitch division lithography offers higher resolution but also faces significant challenges such as added cost and tighter process control. Several process schemes are proposed and compared in terms of complexity, susceptibility to alignment error and CD uniformity control. It is shown that the overlay budget does not necessarily decrease compared to double patterning. The main challenge in higher order pitch division comes from controlling the key processing steps that directly form lines or spaces. In addition, line CD control is easier than space (gap) control in all four "positive-tone" processes studied, similar to the double patterning case. Among the proposed processes, a freezing assisted double spacer (FADS) process that is simpler than the common sidewall spacer approach shows promise for balanced process control.

Keywords: Pitch-division, double patterning, triple patterning, manifold patterning

1. INTRODUCTION

The extensive CD scaling in lithography has been enabled by wavelength reduction, resolution enhancement techniques (RETs) and immersion lithography. Along the road, double-patterning lithography, extreme ultraviolet (EUV) lithography and high index liquid (HIL) lithography are undoubtedly the most significant ones among the latest efforts made. While double patterning is favored for the 32nm node, the battle between double patterning and EUV continues on for 22nm and even 16nm node. Beyond 16nm node, it is not clear which technology is advantageous. Double patterning is not applicable to 16nm node and beyond with current NA (1.35). EUV is now targeted for the 16nm node but requires higher NA to continue the scaling.

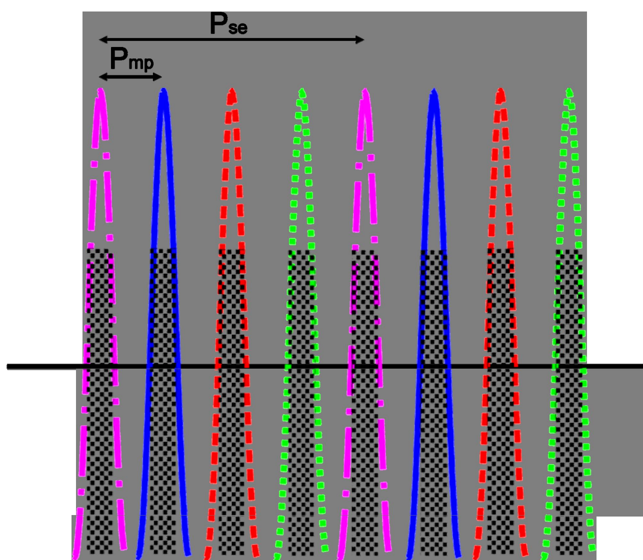

Figure 1. Illustration of pitch division by manifold patterning. Aerial image with intensity above the threshold is recorded in the photoresist. Subsequent exposures are done by shifting the mask $1/N^{th}$ of the original pitch. In this example, four times pitch division is made by quadruple patterning.

Optical Microlithography XXII, edited by Harry J. Levinson, Mircea V. Dusa, Proc. of SPIE Vol. 7274,
72741Y · © 2009 SPIE · CCC code: 0277-786X/09/$18 · doi: 10.1117/12.816131

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As we have seen again and again, the semiconductor industry seems to favor optical lithography as long as it is viable. At 16nm node and beyond, one possible solution is higher order pitch division, *i.e.* manifold patterning (MP), which is a natural extension to double patterning optical lithography. Despite the added cost and complex process, higher order pitch division offers higher resolution with a capable photoresist. In each patterning step, only the minimum resolution information is used. The final pattern is the assembly of the carefully placed lines (or spaces) of N patterning steps. The smallest pitch the system can produce is N times the minimum resolution and is governed by factors such as process window or resist printability. This is shown in Figure 1. It is the objective of this paper to explore the process schemes for higher order pitch division and analyze their process complexity, overlay requirement and CDU budget.

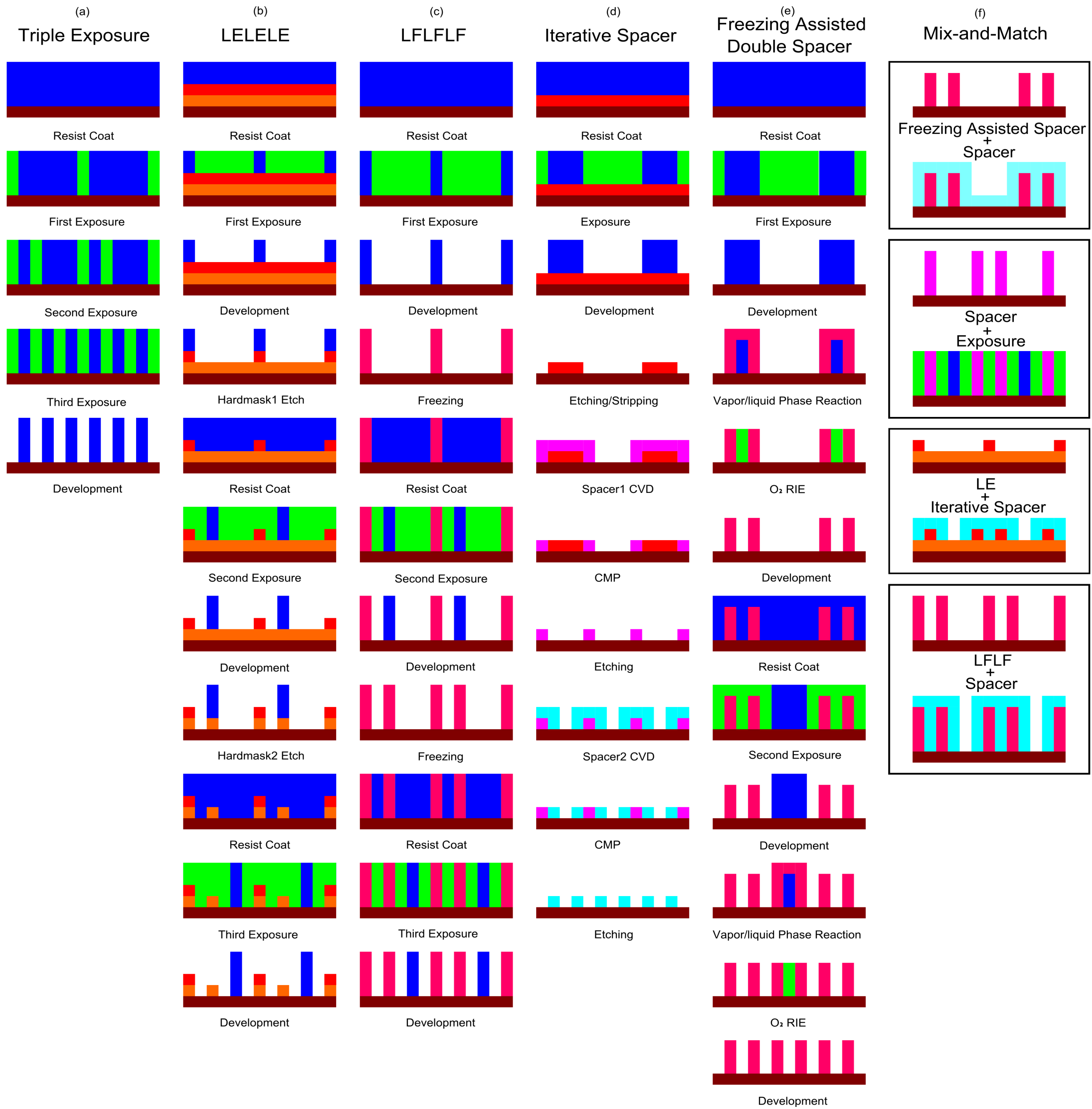

Figure 2. Detailed process schemes for higher order pitch division. a-c. triple patterning including triple exposure, LELELE and LFLFLF; d-e. quadruple patterning including iterative spacer and freezing assisted double spacer; f. mix-and-match process.

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2. HIGHER ORDER PITCH DIVISION LITHOGRAPHY

Most double patterning techniques are generally extendable to higher order pitch division. Therefore, it is possible to adopt a mix-and-match approach to construct a manifold patterning process. Figure 2 shows a list of process flows aiming at triple patterning or quadruple patterning. The simplest form of triple patterning is triple exposure (Figure 2a) which requires a nonlinear photoresist. Possible candidates include contrast enhancement layer (CEL)[1] and two-photon absorption materials[2]. Figure 2b shows the logic extension of the litho-etch-litho-etch (LELE)[3] to litho-etch-litho-etch-litho-etch (LELELE). In this process, at least two hardmasks with good etch selectivity are required for pattern transfer. Additional hardmasks may be needed for CDU control. Similarly, Figure 2c shows extension from the litho-freeze-litho-freeze (LFLF)[4] to litho-freeze-litho-freeze-litho-freeze (LFLFLF). While the freezing process typically causes CD change, tight control is placed on different CD populations. Iterative spacer (Figure 2d) is a succession of the self-aligned sidewall spacer technology[5]. After the formation of the first spacer pattern, another layer of spacer material is deposited on top and forms a new spacer pattern with a total four times pitch division. By using a multi-tiered hardmask approach, Carlson and Liu[6] have demonstrated successful pitch division from 1.2μm to 80nm by three iteration spacer lithography. Figure 2e shows an innovative freezing assisted double spacer (FADS) process. Upon vapor/liquid phase reaction (VLPR) in a track compatible reaction chamber, the freeze material cross-links with both the sidewall and the top portion of the exposed pattern. The thickness of the reacted portion of the pattern is dependent on the freeze material, flow rate, bake temperature and time. A subsequent oxygen reactive ion etch (O_2 RIE) step will first remove the top portion of the photoresist, leaving the un-reacted photoresist exposed by the excessive photons inside the RIE chamber. After removing the exposed photoresist, the crosslinked sidewall could then act as an etch mask for pattern transfer. Repeating the process with an interdigitating mask allows for patterns between two groups of spacers, leading to quadruple patterning. The process is simplified over more common sidewall spacer approaches by replacing the etch-CVD-CMP-etch process with a three-step VLPR-RIE-development process. Potential freeze materials include RELACS[7] and diamines[8]. Figure 2f lists more process schemes which are mixtures of the previously mentioned techniques. For example, common CVD sidewall spacer can be formed on the freezing assisted spacer patterns. This extra degree of freedom offers the opportunity to customize a higher order pitch division process scheme based on the strengths of existing double patterning processes.

3. CD UNIFORMITY ANALYSIS

Similar to the double patterning process, higher order pitch division usually results in multiple CD populations. Assuming a positive tone process, the final line CD uniformity is a combination of N line CD populations. For the spaces, overlay error introduced in the process will manifest itself in the CD error as is evident in the following analysis. The analysis is similar for a negative tone process, except that the effects are reversed for lines and spaces.

In order to understand how individual process steps affect the final CDU, we adopted Nikon CDU model[9] for double patterning and extended it to higher order pitch division. This approach is based on grouping different populations of lines and spaces. The CDU (3σ) of the total line or space pattern is given as the pooled variance of multiple CD populations with different individual means ($\mu_1, \mu_2, \ldots \mu_N$) and standard variations ($\sigma_1, \sigma_2, \ldots \sigma_N$) as:

$$3\sigma_{\text{overall}} = \sqrt{\frac{\sum_{\text{N}} (3\sigma_{\text{N}})^2}{\text{N}} + (3\sigma_{\mu_1\mu_2\cdots\mu_{\text{N}}})^2}\ , \tag{1}$$

where $\sigma_{\mu 1 \mu 2 \ldots \mu N}$ is the standard deviation of the means of N populations. Furthermore, CDU budget is assigned based on educated estimation for 32nm/16nm DRAM half-pitch, given by ITRS 2008 update[10] as 3.3nm/1.7nm.

3.1 LELELE/LFLFLF

Our analysis treats LELELE and LFLFLF as the same process in terms of CDU breakdown. The detailed etch or freezing effects are buried into the parameters defined below:

CD of line 1: L_1 (mean: CD_1; 3σ: ΔCD_1) overlay of line 1: ovl_1 (mean: OL_1; 3σ: ΔOL_1)

CD of line 2: L_2 (mean: CD_2; 3σ: ΔCD_2) overlay of line 2: ovl_2 (mean: OL_2; 3σ: ΔOL_2)

CD of line 3: L_3 (mean: CD_3; 3σ: ΔCD_3) overlay of line 3: ovl_3 (mean: OL_3; 3σ: ΔOL_3)

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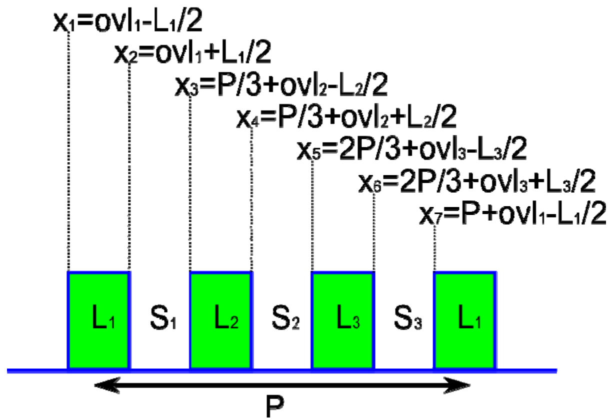

Figure 3. Edge coordinate definitions for LELELE/LFLFLF process.

	Estimated budget (nm)	Line (nm)	Space (nm)
ΔCD	2.5/1.3	2.7/1.5	3.3/1.7
$3\sigma_{CD_1,CD_2,CD_3}$	1.2/0.7		
ΔOL	1.6/0.9		
$3\sigma_{\overline{S_1},\overline{S_2},\overline{S_3}}$	1.6/0.7		

Figure 4. CDU budget for LELELE/LFLFLF process (32nm/16nm half-pitch).

Assuming the CD uniformity and the standard deviation of the individual overlay are the same for each patterning step, *i.e.* $\Delta CD_1=\Delta CD_2=\Delta CD_3=\Delta CD$, $\Delta OL_1=\Delta OL_2=\Delta OL_3=\Delta OL$, the width of each line is of the same standard deviation ΔCD and respective means of CD_1, CD_2, and CD_3. The CDU for lines is expressed as:

$$\Delta CD_{line} = [\Delta CD^2 + (3\sigma_{CD_1,CD_2,CD_3})^2]^{1/2}. \tag{2}$$

For spaces, three overlay dependent populations exist. The edge coordinates are shown in Figure 3. The width of each space is expressed as:

$$S_1 = \frac{P}{3} + ovl_2 - ovl_1 - \frac{L_2}{2} - \frac{L_1}{2},$$

$$S_2 = \frac{P}{3} + ovl_3 - ovl_2 - \frac{L_3}{2} - \frac{L_2}{2}, \text{ and}$$

$$S_3 = \frac{P}{3} + ovl_1 - ovl_3 - \frac{L_1}{2} - \frac{L_3}{2}. \tag{3}$$

The resultant CDU for spaces is expressed as:

$$\Delta CD_{space} = \left[2\Delta OL^2 + \frac{\Delta CD^2}{2} + (3\sigma_{\overline{S_1},\overline{S_2},\overline{S_3}})^2 \right]^{1/2}, \tag{4}$$

where $\sigma_{\overline{S_1},\overline{S_2},\overline{S_3}}$ is the standard deviation of the means of three space populations. Investigating into the CD error terms in CDU line and space, it is evident that line CD is easier to control and is independent on alignment error. Furthermore, overlay error is still the most significant contributor in space CD control, but the situation is not worse than the double patterning CDU control. The first two weighting factors remain the same for LELELE/LFLFLF triple patterning process. The difference is that one need to level the means of three populations instead of two. In another word, the interaction between exposures needs to be minimum, whether it's etch induced or freezing induced CD change.

In addition, CDU budget is assigned for line and space control to achieve a final space CDU of 3.3nm/1.7nm, as specified on ITRS 2008 update for 32nm/16nm DRAM half-pitch. This is shown in Figure 4. Since we are targeting 16nm as the possible introduction node for triple patterning, nearly all requirements for double patterning needs to be

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twice as tight. Although no current known exposure tools are capable to meet those requirements, the CDU specs scaling is linear with regard to CD scaling. Technology innovation is needed for this process to be legitimate.

3.2 Iterative spacer

In the case of iterative spacer process, the lines and spaces are defined by the sidewall spacers. Similarly, we define the exposure and two deposition processes with the following characteristics:

CD of line: L_{litho} (mean: CD_{litho}; 3σ: ΔCD_{litho})

overlay of line: ovl_{litho} (mean: OL_{litho}; 3σ: ΔOL_{litho})

width of spacer 1: L_{sp1} (mean: CD_{sp1}; 3σ: ΔCD_{sp1})

width of spacer 2: L_{sp2} (mean: CD_{sp2}; 3σ: ΔCD_{sp2})

It is evident from Figure 5 that the lines are solely defined by the second spacer, similar to the double patterning spacer process where the final lines only depend on the (first) spacer. Therefore, the line CDU can be expressed as:

$$\Delta CD_{line} = \Delta CD_{SP2}. \tag{5}$$

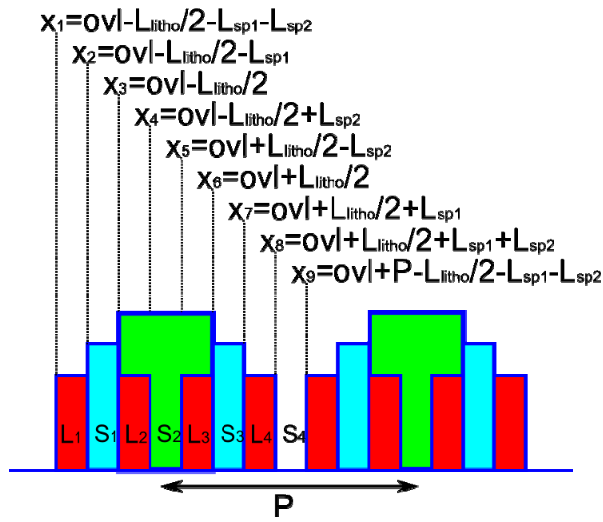

Figure 5. Edge coordinate definitions for iterative spacer process.

	Estimated budget (nm)	Line (nm)	Space (nm)
ΔCD_{litho}	2.5/1.3		3.3/1.7
ΔCD_{sp1}	1.1/0.6	1.5/0.8	
ΔCD_{sp2}	1.5/0.8		
$3\sigma_{\overline{S_1},\overline{S_2},\overline{S_3},\overline{S_4}}$	1.2/0.5		

Figure 6. CDU budget for iterative spacer process (32nm/16nm half-pitch).

The calculation is more complicated for spaces. Four space CD populations exist and each is given by the following expression, respectively:

$$S_1 = L_{sp1},$$

$$S_2 = L_{litho} - 2L_{sp2},$$

$$S_3 = L_{sp1}, \text{ and}$$

$$S_4 = P - L_{litho} - 2L_{sp1} - 2L_{sp2}. \tag{6}$$

The final space CDU of a two iteration spacer process is

$$\Delta CD_{space} = \left[\frac{\Delta CD_{litho}^2}{2} + \frac{3\Delta CD_{sp1}^2}{2} + 2\Delta CD_{sp2}^2 + (3\sigma_{\overline{S_1},\overline{S_2},\overline{S_3},\overline{S_4}})^2 \right]^{1/2}, \tag{7}$$

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where $\sigma_{\overline{S_1},\overline{S_2},\overline{S_3},\overline{S_4}}$ is the standard deviation of the means of four space populations given in equation (6). Overlay error is not included in the CDU model so the iterative spacer process is still self-aligned. The second spacer formation is certainly a key process which not only defines the linewidth but also weighs heavily on space CD uniformity. Even though good CD uniformity (~1.1nm)[5] has been achieved on single spacer formation using a multiple hardmask transfer approach, direct spacer on spacer formation may prove to be difficult because of the tilted spacer profile. One possible solution is to transfer the first spacer pattern into an underline hardmask for subsequent deposition.

Similarly, the CDU budget for the iterative spacer process is described in Figure 6. The litho requirement is assumed the same for the LELELE/LFLFLF process. Stringent requirement is placed on the first and second spacer deposition process where sub 1nm uniformity is needed for 16nm node. Experimental results need to be obtained to evaluate the feasibility of the process. In addition, like any spacer process, an additional trimming mask is needed to open the line-end bridging.

3.3 Freezing assisted double spacer

Freezing assisted double spacer process includes two exposures and two surface freezing steps. Similarly, we define the process with the following key parameters:

CD of line 1: L_1 (mean: CD_1; 3σ: ΔCD_1)

CD of line 2: L_2 (mean: CD_2; 3σ: ΔCD_2)

overlay of line 1: ovl_1 (mean: OL_1; 3σ: ΔOL_1)

overlay of line 2: ovl_2 (mean: OL_2; 3σ: ΔOL_2)

freezing depth: d_{fr} (mean: D_{fr}; 3σ: ΔD_{fr})

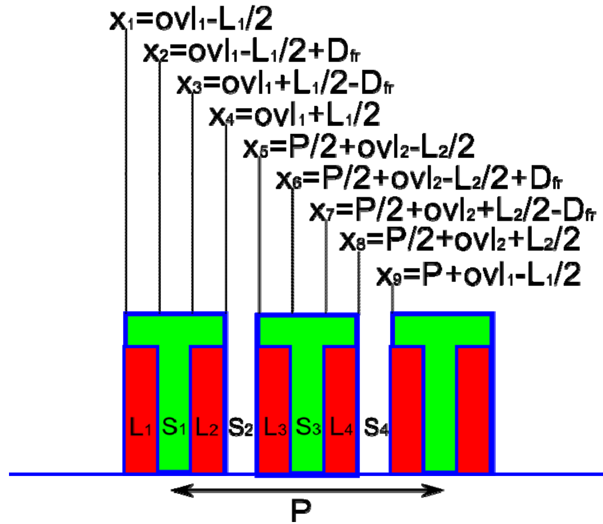

Figure 7. Edge coordinate definitions for freezing assisted double spacer process.

	Estimated budget (nm)	Line (nm)	Space (nm)
ΔCD	2.5/1.3		3.3/1.7
ΔOL	1.6/0.9		
ΔD_{fr}	1.2/0.5	1.2/0.5	
$3\sigma_{\overline{S_1},\overline{S_2},\overline{S_3},\overline{S_4}}$	0.9/0.5		

Figure 8. CDU budget for freezing assisted double spacer process (32nm/16nm half-pitch).

As shown in Figure 7, the line CD depends only on the surface freezing depth and the line CDU is given as:

$$\Delta CD_{line} = \Delta D_{fr} . \tag{8}$$

For spaces, four CD populations also exist and are given in the following expression:

$$S_1 = L_1 - 2d_{fr} ,$$

$$S_2 = \frac{P}{2} + ovl_2 - ovl_1 - \frac{L_1}{2} - \frac{L_2}{2} ,$$

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$$S_3 = L_2 - 2d_{fr}, \text{ and}$$

$$S_4 = \frac{P}{2} + ovl_1 - ovl_2 - \frac{L_1}{2} - \frac{L_2}{2}. \quad (9)$$

Assuming the CD uniformity and the standard deviation of the individual overlay are the same for each patterning step, *i.e.* $\Delta CD_1=\Delta CD_2=\Delta CD$, $\Delta OL_1=\Delta OL_2=\Delta OL$, the final space CDU of a two iteration spacer process is

$$\Delta CD_{space} = \left[\frac{3\Delta CD^2}{4} + \Delta OL^2 + 2\Delta D_{fr}^2 + (3\sigma_{\overline{S_1},\overline{S_2},\overline{S_3},\overline{S_4}})^2 \right]^{1/2}, \quad (10)$$

where $\sigma_{\overline{S_1},\overline{S_2},\overline{S_3},\overline{S_4}}$ is the standard deviation of the means of four space populations given in equation (9). Final space CDU model shows complicated dependence on multiple factors such as overlay, litho defined CD uniformity and the surface freezing depth. The surface freezing process is identified as the key process as it consumes most of the space CDU budget and defines the linewidth. Similarly, an additional trimming mask is needed to open the line-end bridging. The CDU budget for the freezing assisted double spacer process is described in Figure 8. The litho and overlay requirements are assumed to be the same as the LELELE/LFLFLF process. Sub 1nm freezing depth uniformity is required for 16nm node.

Even though such complicated CD error distribution may be hard to control, it gives an example of how one can mix the existing double patterning processes to construct a higher order pitch division process with acceptable CDU. If the LELELE/LFLFLF process proves to be difficult because of the tight overlay budget, the freezing assisted double spacer process trades off some freezing process budget for overlay budget. If the iterative spacer process proves to be impractical because of the strict requirement on two spacers, this process trades off some overlay budget for relaxed deposition/freezing process. More processes can be constructed and evaluated using the similar approach.

4. CONCLUSIONS

Lithographers are understandably cautious of higher order pitch division or manifold patterning process because of the potential high cost and process complexity. However, it is still worthwhile to look into this option as it is the most straightforward way to continue far field optical lithography. As we get closer to the atomic limit of resolution, such techniques requires the least amounts of investment in constructing the infrastructure.

This paper studies the feasibility of higher order pitch division from a CD uniformity viewpoint. Even though the proposed processes face significant engineering challenges, several conclusions can be drawn from the analysis:

1) In general, overlay budget is not tightened in higher order pitch division processes compared to the double patterning scenario.
2) If we are able to control the key process steps in double patterning, much of the efforts in designing higher order pitch division process are to linearly scale the technology into the next generation. No tighter requirement is placed on the higher order pitch division process itself.
3) The strength of higher order pitch division is the possibility of mix-and-match existing double patterning techniques to achieve acceptable process control.

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